DETAILED ACTION

In light of the interview with Mr. Eric M. Shelton on 3/9/2009, the final rejection sent on 12/10/2008 has been vacated and prosecution in case 10/585,643 has been reopened.

The instant application having Application No. 10/585,643 has a total of 18 claims pending in the application, there are 18 independent claims and 0 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6, 12, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiba (US 6,401,166).

Regarding Claim 6, Chiba teaches a non-volatile semiconductor recording medium **(flash memory 1 of Figure 1)** in which information is recorded according to a recording format of FAT file system **(Chiba uses the FAT file system, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

wherein a user data region comprising a plurality of clusters **(data regions of Figure 4, which also shows a plurality of clusters among the data regions)** and a file allocation table region **(FAT region of Figure 4)** are included in the FAT file system;

an information on a state of each cluster in the user data region is recorded in the file allocation table region **(since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT inherently records information on the state of the clusters, Column 14 Lines 3-4)**;

the file allocation table region indicates that a continuous series of at least three clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster or an already-used cluster **(the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if three continuous clusters are used, the file allocation table region would indicate that a continuous series of at least three clusters are used)**,

and a region of the user data region corresponding to the continuous series of at least three clusters is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25)**.

Claim 12 is the method equivalent to Claim 6, and is rejected under similar rationale.

Claim 18 is the information recording format equivalent to Claim 6, and is rejected under similar rationale.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7, 9, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by **Chiba (US 6,401,166) in view of Briner et al (US 6,591,327).**

Regarding Claim 1, Chiba teaches a recording medium of non-volatile semiconductor **(flash memory 1 of Figure 1)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**;

a partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)** and

a partition region **(starting with partition boot memory region of Figure 4)**, wherein

an information on a start position of the partition region is recorded in the partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**,

the start position information includes a value at which a predetermined region **(the predetermined region being the "empty region" of Figure 4)** is secured between a terminal end of the partition management information region and a starting end of the partition region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition [including the empty region] begins and ends, Column 8 Lines 27-32)**, and

the region secured between the terminal end of the partition management information region is larger than the first size **(Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)** and the starting end of the partition region is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to units within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 3, Chiba teaches a non-volatile semiconductor recording medium **(flash memory 1 of Figure 1)** comprising:

a plurality of erasing blocks, each erasing block being of a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**; wherein

information is recorded according to a recording format of a predetermined file system **(FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

a region which is not used for the recording is larger than the first size included in the recording format of the file system **("empty region" of Figure 4, which is used "for coinciding a head and end of the block...with those of a cluster", and is thus not used for the recording, Column 8 Lines 34-38, also Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)**, and the region which is not used for the recording is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in**

a state where data is physically erased).

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Claim 7 is the method equivalent to Claim 1, and is rejected under similar rationale.

Claim 13 is the information recording format equivalent to Claim 1, and is rejected under similar rationale.

Claim 9 is the method equivalent to Claim 3, and is rejected under similar rationale.

Claim 15 is the method equivalent to Claim 3, and is rejected under similar rationale.

Claims 5, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba in view of Nakamura et al (US 6,873,789).

Regarding Claim 5, Chiba teaches a non-volatile semiconductor recording

medium of non-volatile semiconductor **(flash memory 1 of Figure 1)** comprising:

a partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

and a partition containing a file system specific region **(Chriba uses the FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32)**,

the partition comprises a partition descriptor information region **(partition boot memory region of Figure 4)**;

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

the start position information includes a value at which a predetermined region of a plurality of memory blocks **("empty region" of Figure 4, composed of multiple pages [blocks] of memory as shown on Figure 4)** is secured prior to a starting end of the file system specific region region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this**

memory", Column 8 Lines 21-26), and

the region secured prior to the starting end of the space bit map region **(the empty region is shown between the boot information region and file allocation table region in Figure 4)** is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chriba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system **(Column 6 Lines 22-25)** with a space bit map in memory **(Column 12 Lines 52-53)**. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used the space bit map for the file system specific region of Chriba and to use a UDF file system in place of the FAT file system, so that the memory device of Chriba can be compatible with operating systems that use the UDF file system.

Claim 11 is the method equivalent to Claim 5, and is rejected under similar rationale.

Claim 17 is the information recording format equivalent to Claim 5, and is rejected under similar rationale.

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

SUBJECT MATTER CONSIDERED ALLOWABLE

Claims 2, 8, 14, 4, 10, and 16 have been considered allowable subject matter.

The primary reason for allowance of **Claims 2, 8, and 14** rest in the combination with the inclusion of the following limitation of:

"the second and third address values are not consecutive, and are separated by at least three consecutive address values corresponding to a switch region located between the first and second partition regions; and the switch region is physically erased".

The primary reason for allowance of **Claims 4, 10, and 16** rest in the combination with the inclusion of the following limitation of:

"the reserved sectors being positioned in the partition between the partition boot information region and a starting end of the file allocation table region".

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 3, 5, 6, 7, 9, 11, 12, 13, 15, 17, and 18 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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